A High-Precision Direct-Reading Loss and Phase Measuring Set for Carrier Frequencies

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A set has been developed to measure the parameters of insertion loss and phase shift of communication systems components. The design effort has been directed toward achieving laboratory precision in measurement and at the same time maintaining the ease of use and speed necessary for a large volume of measurements. Accuracies of ±0.002 db, ±0.02 degree and ±1 cycle have been attained over the frequency range from 10 to 300 kc. The entire frequency range is covered without band switching by the use of a heterodyne signal oscillator which provides frequency accuracy by locking to a frequency standard. The principle of phase detection is based on measurement of the time interval corresponding to the displacement of sine wave zero crossings caused by the unknown. This method has the advantage of good accuracy inherent in the measurement of time by counting techniques and also the ease of automatic readout of phase shift by translation from time units. In measuring loss, use of a rapid sampling technique to compare the unknown with a standard eliminates errors caused by circuit drifts.

The ever increasing complexity of communication systems and the demand for high-quality transmission have emphasized the need for close control of system components such as filters, equalizers, and repeaters. Precise instrumentation to measure the parameters of loss and phase shift must be provided for use in both the development and production areas of these components.

In the case of broadband carrier systems this need was met by development of a 3.6 mc phase measuring set.[1] Later, the set was modified to provide increases in maximum frequency from 3.6 to 20 mc, loss measurement accuracy from ±0.05 to ±0.02 db and phase measurement accuracy from ±0.25 to ±0.1 degree.

The need for instrumentation to control components in the case of

high-speed data systems has been met by the recent development of a 10 to 300 kc phase measuring set. This set will automatically measure and read out insertion phase shift to an accuracy of 0.02 degree and will measure insertion loss to an accuracy of 0.002 db.

The performance specifications of the new set are more completely stated as follows:

Frequency: 10 to 300 kilocycles; maximum accuracy ±1 cycle
Generator and network termination impedance: 75 ohms unbalanced
Test signal level: +6 dbm
Insertion loss range: 0 to 100 db, maximum accuracy ±0.002 db
Insertion phase shift range: 0 to 360°, maximum accuracy ±0.02°

The quantities measured are defined in Fig. 1. Conforming to these definitions, the measuring system compares phase and amplitude of the outputs of two transmission channels energized from the measurement frequency source, one of which serves as a standard channel while the other contains the apparatus under test. This is illustrated in the block diagram of Fig. 2.

The measuring circuit uses the heterodyne principle,[1] which provides the high degree of frequency discrimination required for precision measurements and the ease of operation by self-tuning. Heterodyning also translates the phase of the unknown from the variable frequency to a constant low intermediate frequency at which phase shift can be accurately detected. The principle of phase detection is based on measurement of the time interval corresponding to the displacement of a sine-wave zero crossing caused by the unknown, as discussed in more detail in Section IV. This method has the advantage of good accuracy inherent in the measurement of time by counting techniques and also the ease of automatic readout of phase shift by translation from time units.

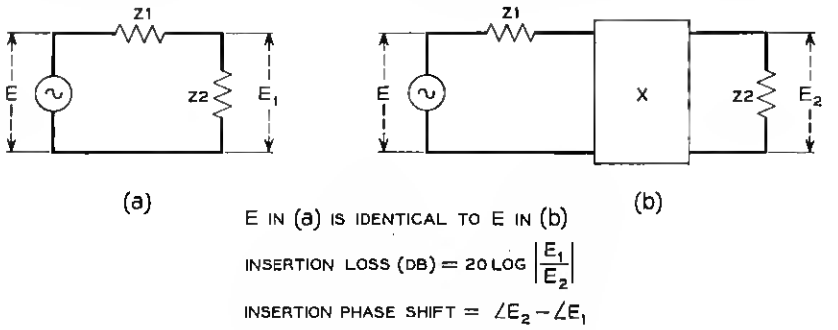

Fig. 1 — Definition of quantities measured.

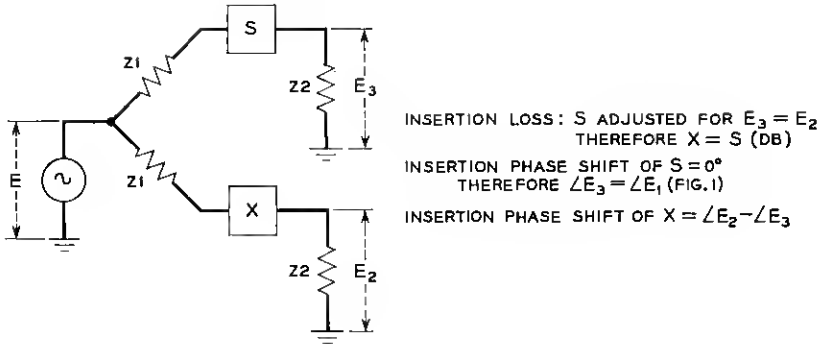

Fig. 2— Basic block diagram.

Alternate connection of the loss detection circuit to the standard and test channels[2, 3] is made at a relatively rapid rate by the use of mercury relays driven at 13 cycles per second. This fast switching method results in minimizing errors caused by magnitude instabilities in the measurement signal source which are prohibitive in manual switching methods. In phase measurements, where magnitude changes are less critical, the alternate connection of the phase detection circuit to the two channels is made at a slower rate to allow for an accurate measure of time. The overall circuit is illustrated in two sections by the block diagrams of Figs. 3 and 4.

For loss measurements a single master switch sets up the connection of Fig. 3 and the timed driving voltages for the switches. The signal at frequency F is applied through both the standard and unknown channels of the comparison unit, whose outputs are connected alternately to the input of a wideband amplifier. Approximately equal detection sensitivity for various values of loss of an unknown is attained automatically by ganging the amplifier gain controls to the standard attenuator control switches so that the level of the signals supplied to the detector is maintained constant to within 1 db. The loss detector then compares the magnitudes of the two signals and indicates their inequality on its meter. When the attenuator is adjusted for zero meter reading, the loss of the unknown is read directly from the attenuator dials. Details of the loss detection system are given in Section III.

For phase measurements, the master switch automatically connects the constant phase attenuator in place of the loss attenuator, connects the output signals of the two channels to the phase detector in place of the loss detector, as shown in Fig. 4, and changes the timing of the circuit

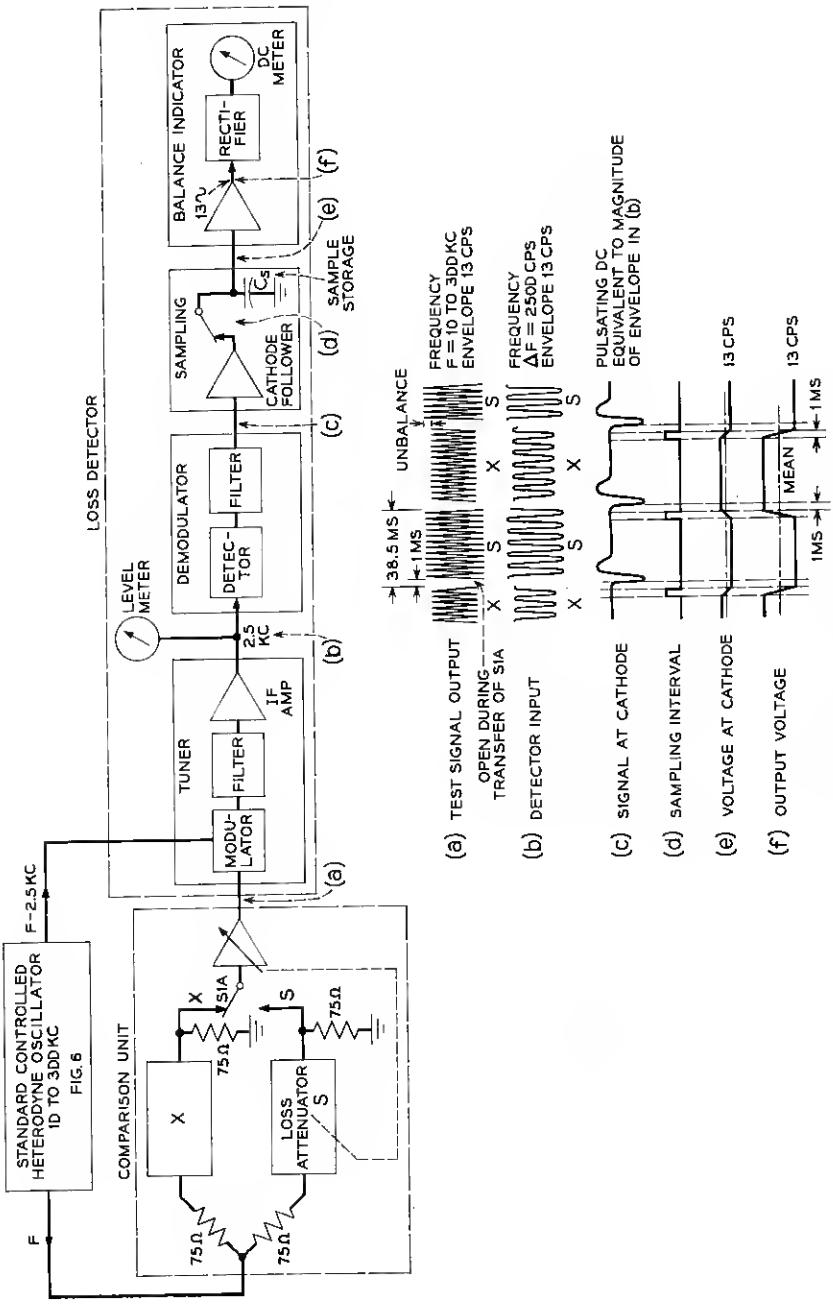

Fig. 3 — Block diagram of loss measurement circuits.

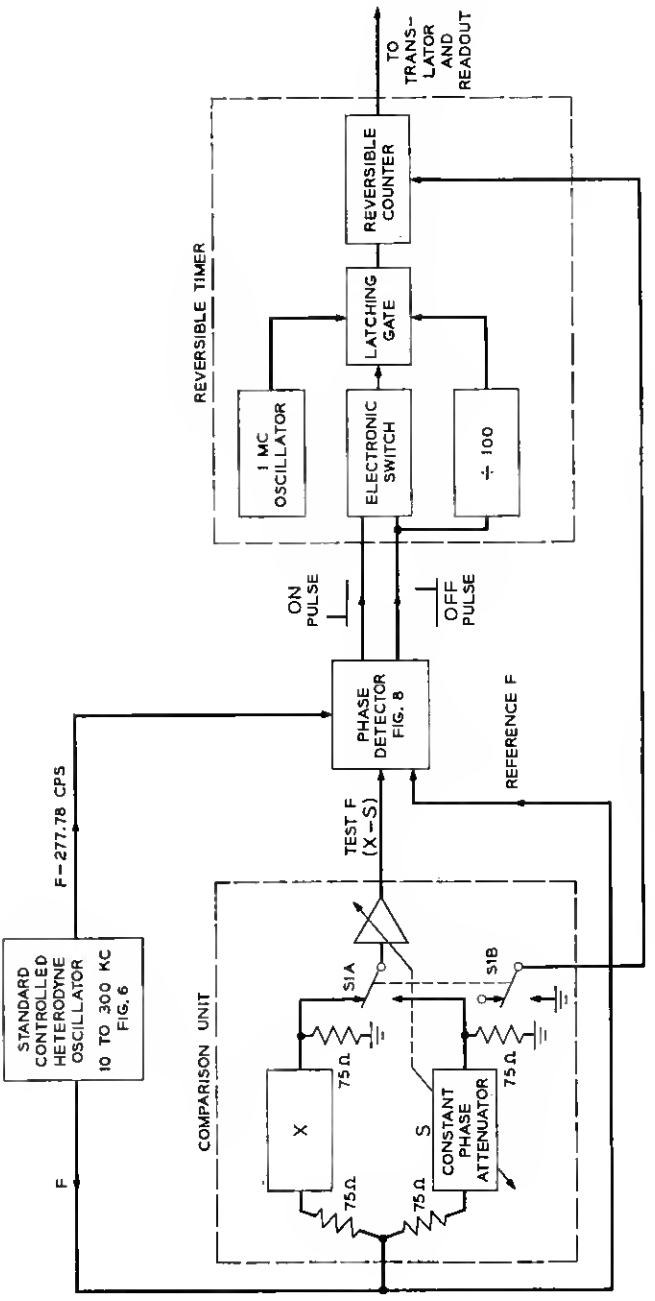

Fig. 4 — Block diagram of phase measurement circuits.

relays. The difference in phase of the two signals is now detected and indicated on an in-line readout. The constant phase attenuator is compensated so that at any setting it introduces phase shift in the standard arm exactly equal to the phase shift in the unknown arm for "zero" setting, i.e., with a patch cord inserted in place of the unknown. The indicated phase is thereby the phase shift due to insertion of the unknown. Ganging of the constant phase attenuator to the loss attenuator automatically maintains the magnitude equality of the loss measurement and thereby eliminates possible errors in phase detection due to unequal signal magnitudes. The details of the phase-detection system are also described below.

I. MEASURING SET DESIGN

The component chassis of the set are mounted in a console assembly of three relay rack cabinets as shown in Fig. 5. Particular emphasis has been placed on the arrangement of the chassis in the cabinets so that the controls of oscillators F1 and F4 and of the comparison units, which are the ones that are operated in the normal measurement procedure, are within easy reach of a seated operator. The loss balance, phase, and level indicators are also located for ease of viewing. Accessibility to chassis maintenance test points and to components for replacement is provided by mounting the most critical chassis on sliding and tilting chassis tracks. Access to rigidly mounted chassis is permitted through rear cabinet doors and in some instances through hinged front chassis covers.

The function of the individual units in relation to the overall circuit and some of the significant design considerations are discussed under the following headings:

II. STANDARD CONTROLLED HETERODYNE OSCILLATOR (SCHO)
III. LOSS DETECTOR
IV. PHASE DETECTOR
V. REVERSIBLE TIMER
VI. COMPARISON UNIT

II. STANDARD CONTROLLED HETERODYNE OSCILLATOR (SCHO)

The SCHO is the most complex part of the measuring set and includes seven separate units. Six units occupy the complete upper part of the left-hand bay and one unit is at the top of the central bay as shown in Fig. 5

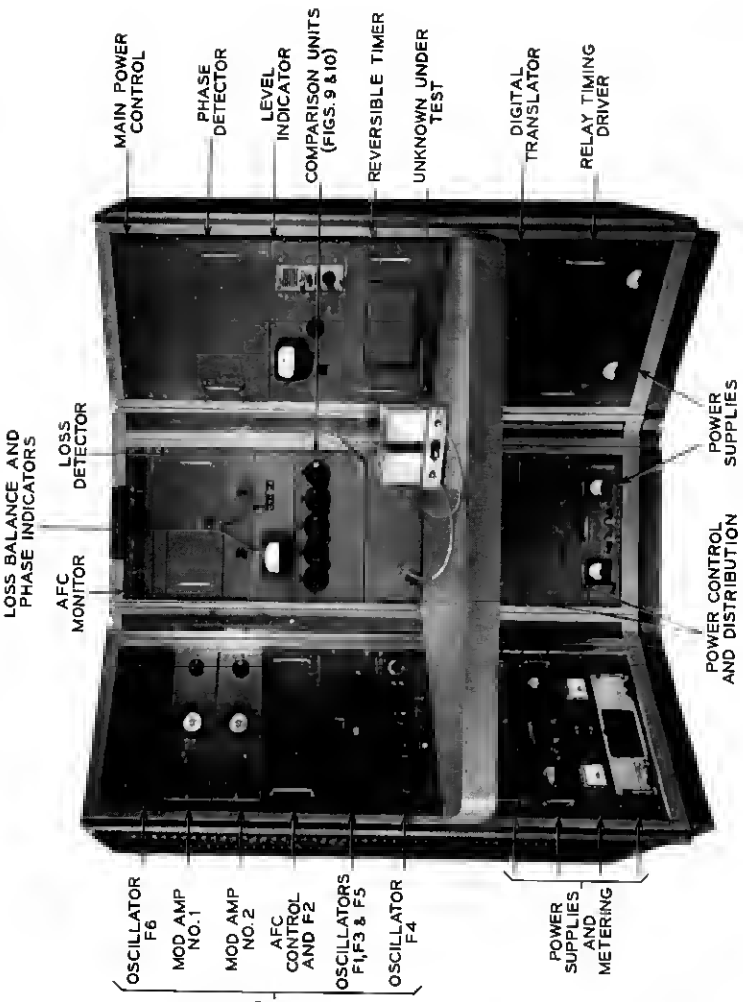

Fig. 5 — The assembled loss and phase measuring set.

It is found convenient to treat the discussion of the SCHO under the following sub-headings:

2.1 General Description and Requirements of the SCHO
2.2 Functions of Automatic Frequency Control (AFC) Loops
2.3 Design Considerations of AFC Loops

2.1 *General Description and Requirements of the SCHO*

The need to accurately measure the characteristics of networks having steep transmission and phase slopes prescribes stringent frequency accuracy requirements on the oscillator. To obtain an accuracy of ± 0.002 db in the presence of a 2 db per kilocycle slope, a frequency accuracy of ± 1 cps must be maintained. To apply the heterodyne principle, the oscillator must provide dual output frequencies: the test frequency and a slave or offset frequency equal to the test frequency minus a constant (Δ).

The design of the oscillator for this set is based on the principles of a high frequency standard controlled heterodyne oscillator (SCHO).[4] While the SCHO is a complex structure, the setting of the test signal to any desired frequency in the range of 10 to 300 kc accurate to ± 1 cycle is a simple process. The film scale is rotated to the 1 kc mark below the desired frequency and the dials of the four decades of the interpolation oscillator are set to the remaining digits of the desired frequency.

Essentially the oscillator employs local oscillators that can be set to produce the desired test and offset frequencies. These are then automatically and continuously maintained to the desired precision by reference to three standard frequency sources, two internal and one external, as shown in Fig. 6. The output frequencies, F and $F - \Delta$, are generated by a variable oscillator, F1, and two controlled oscillators, F3 and F5. F is the beat between F1 and F3 while $F - \Delta$ is the beat between F1 and F5. These beats are produced in modulator amplifiers 1 and 2 respectively.

As explained below in more detail, the frequency of F is controlled to a multiple of the external 1 kc standard through an intermediate controlled oscillator, F2. The frequency of F is then shifted to the required exact frequency by a variable interpolation oscillator, F4. Finally, the offset frequency is produced by fixed oscillators, F6 or F6′, of the appropriate Δ frequency which control the frequency difference between F3 and F5.

F1 is a stable tuned-grid oscillator[4] with a film scale 100 inches in length calibrated in terms of F at every 10 kc and further subdivided every 1 kc.

F2, F3 and F5 are tuned-grid reactance tube[1] controlled oscillators.

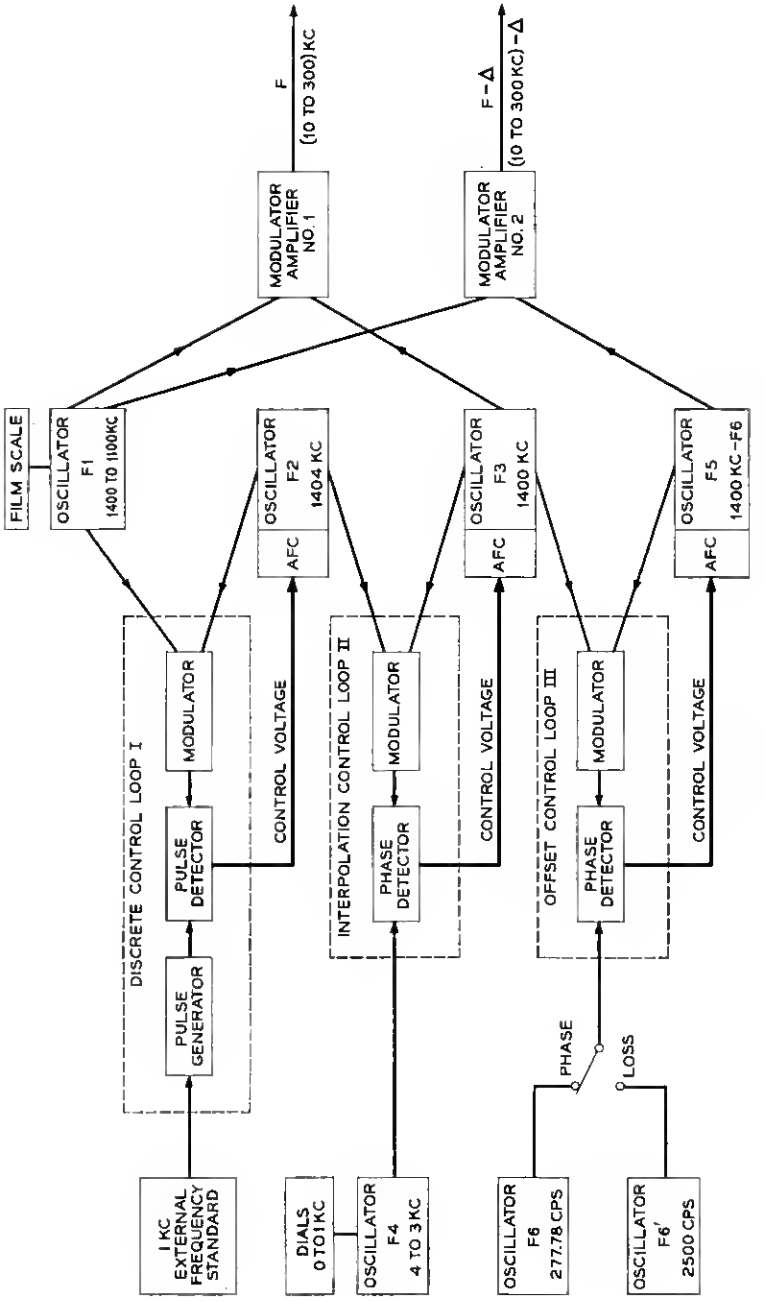

Fig. 6 — Block diagram of standard controlled heterodyne oscillator (SCHO).

F4 is a precision RC decade oscillator.

Oscillator F6 is a tuning fork oscillator, while F6′ is a crystal type. The need for the use of the two offset or Δ frequencies is discussed in Sections III and IV.

2.2 *Functions of Automatic Frequency Control (AFC) Loops*

The discrete control loop I provides voltage to control the frequency of oscillator F2 by using the 1 kc standard as a reference. F2 is controlled so that the difference F2 − F1 is an exact multiple of 1 kc. As F1 is set to within ±200 cps of any 1 kc multiple, as indicated by its calibrated film scale, F2 is shifted in frequency and phase locked to F1 by loop I as required.

The interpolation control loop II provides voltage to control the frequency of oscillator F3 by using the interpolation oscillator F4 as a reference. F3 is controlled so that the difference (F3 − F1) is the chosen 1 kc multiple plus an amount 0 to 1 kc determined by the dial settings of oscillator F4.

The offset control loop III provides voltage to control the frequency of oscillator F5 by using oscillator F6 or F6′ as a reference. F5 is controlled so that the difference F3 − F5 is equal to the frequency, Δ, of the chosen reference oscillators: F6 = 277.78 cps or F6′ = 2500 cps. Since the offset output is F5 − F1, it is equal to (F3 − Δ) − (F3 − F) or F − Δ.

2.3 *Design Considerations of AFC Loops*

Modulation requirements of the SCHO oscillator are severe for both loss and phase measurements. For loss measurement errors not to exceed 0.001 db, amplitude modulation must be held to −80 db. Frequency modulation due to the operation of loop III introduces errors in phase measurement in a more complex manner. Addition of sideband frequencies to the F and F − 277.78 cycle signals fed to the modulators of the phase detector (block diagram in Fig. 7) will introduce a spurious 277.78 cycle signal in the modulator outputs. This spurious signal produces error by shifting the zero crossings, the error reaching a maximum for a 90° phase shift of the spurious component. To meet the circuit objective of 0.01 degree, the level of this interference must be 75 db down.

One source of this interference may be by frequency modulation of F5 of Fig. 6 due to insufficient filtering in loop III. This would allow transmission of frequencies Δ (277.78 cps) and 2Δ (555.56 cps) from the phase detector of loop III, Fig. 6, to the grid of the reactance tube that controls

oscillator F5. The maximum amplitude of this modulating voltage (v_m) must be less than 40 microvolts as shown in the Appendix. This low value prescribes complete, high quality shielding between the components of the frequency control circuitry of loop III and adequate filtering in the loop without introducing excessive delay.

From the description of loop functions, it will be seen that F5 must change in frequency by at least 1.5 kc, since it must compensate for frequency drifts of the order of 0.5 kc in F1, F2 and F3, as well as cover the 1 kc range of F4. In addition to this wide control range, the offset loop III must maintain the phase difference between the test and offset signals to within 0.01 degree during the phase measurement time interval to meet the objective of circuit accuracy.

The loop includes both frequency discriminating and phase detecting circuits and the reactance tube control of F5. The desired control was attained by careful design of the following factors: (a) the Q and thereby the frequency slope of the discriminator is made as high as possible with readily available components; (b) the reactance tube is operated at the point in its characteristic which produces maximum change in its output capacitance with a minimum change in grid voltage supplied by the phase detector; and (c) added gain is kept at a minimum to prevent loop sing but still sufficient to maintain control.

III. LOSS DETECTOR

The loss detector circuit is illustrated by the block diagram in Fig. 3. The detector is a self-tuned null balance type which produces an output proportional to the difference in loss of the standard and unknown branches of the comparison unit in Fig. 3 with an unbalance sensitivity of 0.001 db. The operation of the detector circuit will be described first and then the factors governing the choice of constants will be considered.

3.1 *Detector Operation*

The envelope of the test signal varies rectangularly in level (a of Fig. 3) as the comparison switch alternately connects the signal from the loss attenuator and unknown branches of the comparison circuit to the loss detector. The variable frequency signals are translated to a 2500 cps fixed intermediate frequency (b of Fig. 3), amplified, and detected with a parabolic detector. The output of the parabolic detector contains a rectangular component (c of Fig. 3), corresponding to the rectangular envelope of the carrier, and the much larger carrier component which is minimized by filtering. The 2500 cps carrier component is about 80 db

greater than the rectangular component produced by an 0.001 db inequality of the S and X signals.

Transients of variable magnitude are superimposed on the rectangular signal (c of Fig. 3) when the comparison switch is closed. Therefore, for true balance information, the output of the filter is sampled for a very short interval (d of Fig. 3) near the end of the dwell time of the comparison switch on each side. The capacitor C_8 in the sampling circuit now contains a rectangular component[2, 3] (e of Fig. 3) at the switching frequency of 13 cycles. The amplitude of this component is proportional to the amount of unbalance between the standard and unknown paths, and the polarity with respect to the mean value is dependent on the sense of unbalance. This signal is then amplified, (f of Fig. 3) rectified, and the rectified voltage applied to a zero center dc meter. The meter deflection is now proportional to the loss unbalance and its direction from mid-scale indicates which of the two signals is the larger and thereby indicates whether the loss of the standard must be increased or decreased to attain balance of the signals. The balance indicator provides a relatively constant deflection for the same loss unbalance in db, independent of the absolute magnitude of loss, by maintaining the level of the input to the detector relatively constant as discussed in Section VI.

3.2 *Detector Constants and Design Considerations*

The choice of intermediate frequency, bandwidth, switching frequency and measurement period is based on the following considerations. The demodulator is a square-law rectifier detector followed by a low pass filter which must (1) transmit a rectangular envelope component, (2) provide a high attenuation to the intermediate frequency, and (3) have a rapidly decaying transient response.

The filter design problem becomes quite difficult for low values of intermediate frequency, so that a high frequency is desirable. However, if a high frequency is chosen, its low order harmonics may fall within the measurement band of 10 to 300 kc. It is difficult to provide sufficient isolation to prevent pickup of these harmonics from the IF amplifiers of the tuner through parasitic paths, such as power supplies or common grounds, back to the wide band amplifiers of the comparison unit or to units of the SCHO. Such pickup would result in measurement errors since wanted and parasitic signals could add in one position of the switch S1A of the comparison unit and subtract in the other position. An intermediate frequency of 2.5 kc was selected as a compromise value. Since only fourth and higher harmonics of 2.5 kc are in the measurement band, sufficient filtering to remove interference is less difficult.

The choice of bandwidth of the intermediate frequency is a compromise between (1) a narrow bandwidth for a bigh degree of frequency discrimination and thereby a high signal-to-noise ratio for good circuit accuracy and (2) a wide bandwidth to allow a fast decay of switching transients and thereby minimize their effect on circuit accuracy. To limit measurement noise below 0.001 db, a signal-to-noise ratio of 80 db is required. Bandwidth was fixed at 600 cps, which resulted in an 86 db ratio at point b of Figure 3 and a decay time of approximately 20 milliseconds.

The choice of switching rate of 13 cps is a compromise between (1) fast speed to minimize level changes of the signal source during comparison of the two paths and (2) slow speed to allow ample time for transient decay and to relax the accuracy requirement of the sampling timing in relation to the comparison time. In addition, the 13 cps rate was chosen to minimize the effect of pickup that could occur at a submultiple of the 60 cps power frequency.

IV. PHASE DETECTOR

It is convenient to divide the discussion of the phase detector into four categories: (a) General description of the principle of phase detection by measurement of time intervals, (b) Operation of the phase detector, (c) Timing of circuit measuring periods, (d) Design considerations and choice of constants.

4.1 *General Description*

As stated in the introduction, the choice of phase detection by the measurement of the time interval corresponding to the displacement of a sine wave zero crossing was based on the inherent accuracy of time measurement and the ease of automatic readout of phase by translation from time units. The circuit of the detector is illustrated by the block schematic of Fig. 7. The detector measures the phase difference between the test and reference signals of Fig. 4.

The problem of phase measurement over a wide frequency range (see Fig. 7) is simplified to the measurement at a fixed frequency by the preservation of phase in a modulation process. The considerations in the choice of 277.78 cps as the fixed frequency and the choice of a 1 megacycle counting rate will be discussed later.

The time interval, beginning with the negative-going zero crossing of the reference signal and ending with the corresponding negative-going zero crossing of the test signal, is proportional to the phase difference

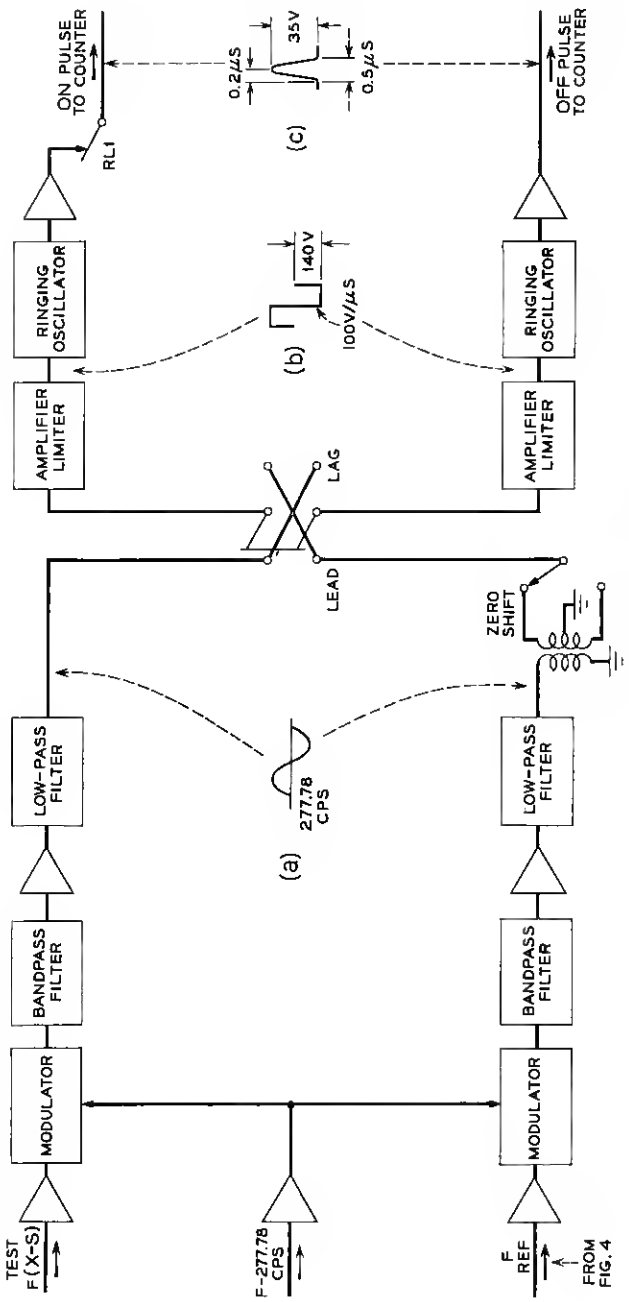

Fig. 7 — Block diagram of phase detector.

between those two channels. Since the time for 360 degree difference equals 1/277.78 second, then 1 microsecond = 0.1 degree and, at a 1 megacyle counting rate, 1 count = 0.1 degree.

Circuit zero errors, due to frequency-variable phase difference between the unknown and reference paths of Fig. 4, are eliminated by the switching of S1 of Fig. 4. The circuit compares the phases of the unknown and reference paths and then compares the phases of the attenuator and reference paths. Since the reference path is common to both comparisons, the resulting measurement is the difference in phase between the unknown and attenuator paths.

4.2 *Description of Detector Operation*

As discussed above, the detector must measure the time interval between negative-going zero crossings of two sine waves. The time of the zero crossings is established by the generation of corresponding sharp pulses at the instant of zero crossing and the time interval between pulses is measured by a reversible timer which is described in Section V.

The IF sine wave of each channel (a of Fig. 7) is clipped and amplified by three limiters in cascade which convert the signal to a fast-rise square wave (b of Fig. 7). The shock-excited triode oscillator is driven to cutoff by the fast negative-going square wave. Oscillations are produced in the tank circuit coil together with its distributed capacitance and a shunt diode damps out all but the first half sine wave. The resultant output pulses (c of Fig. 7) are 0.5 μs wide, 35 volts in magnitude and have a rise time of 0.2 μs. A relay in the ON pulse branch is controlled so that it closes approximately 0.2 second after the X-S switch of the comparison unit closes, thereby closing only after the switching transients have dissipated.

4.3 *Timing of Circuit Measuring Periods*

The direct reading of phase measurement is accomplished by the following sequence of automatic switching as illustrated by the diagram of Fig. 8:

1. The comparison switch S1A of Fig. 4 is switched to X and the timer is switched to "add" by switch S1B. No pulses reach the timer since relay RL1 of Fig. 7 is open.
2. An interval of 0.2 second is allowed for decay of transients introduced by closing S1A.
3. Relay RL1 is closed allowing transmission of pulses to the timer.
4. The timer measures the total time interval of 100 ON-OFF pulses

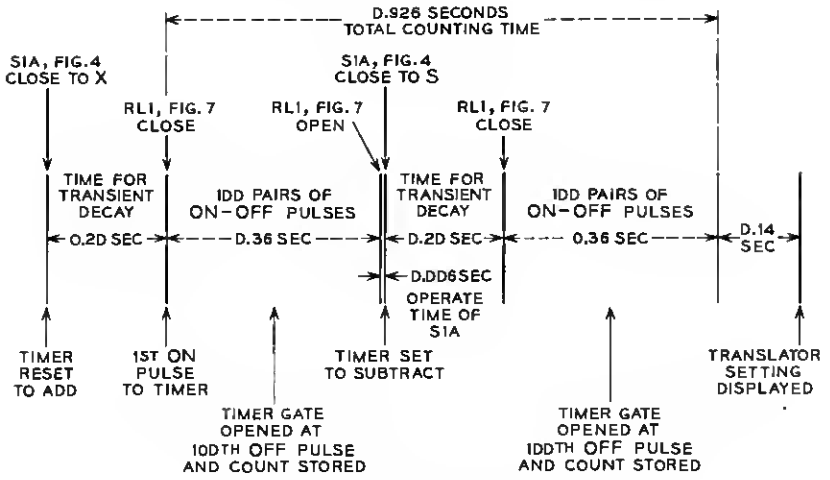

Fig. 8 — Time diagram of phase measurement circuit operation.

from the detector output. The timer gate opens at the 100th OFF pulse and the count is stored. The maximum time (and count) is 0.36 second corresponding to 360 degrees as discussed above.

5. Relay RL1 is again opened.

6. The comparison switch S1A of Fig. 4 is switched to S and the timer is switched to "subtract" by switch S1B.

7. An interval of 0.2 second is allowed for decay of transients.

8. Relay RL1 is closed.

9. The timer measures the total time interval of 100 ON-OFF pulses and subtracts it from the count stored in 4. The timer gate opens at the 100th OFF pulse and the remaining count is stored.

10. After 0.14 second, a relay in a digital translator is closed and the translator setting, corresponding to the stored count of the timer, is displayed by an in-line numerical indicator.

11. After an interval of 2 to 10 seconds, as desired, the entire procedure from 1 to 10 is repeated.

4.4 *Design Considerations and Choice of Constants*

To attain 0.01 degree accuracy of phase measurement, the choice of IF frequency (Δ) in the phase detector, counting rate, and the number of periods measured becomes highly critical because these factors are closely interrelated and also because they are subject to the performance of the SCHO oscillator.

As previously discussed, minimizing errors due to FM modulation

makes the design of the AFC loop III of the SCHO particularly difficult when Δ is small. However, since phase is to be measured by conversion to time, a large Δ requires a high counting frequency (or rate) F_R. Problems of circuit phase "zero," as previously described in Section 4.2, prescribe a reversible counter which is increasingly difficult to design for higher rates. To obtain direct reading phase measurements in decades from 0 to 360 degrees, F_R must be 10^n where n is an integer and $\Delta = F_R/360$. Based on the above considerations, the selected constants were: $F_R = 1.0$ mc and $\Delta = 277.78$ cps from which 1.0 degree = 10 microseconds. Measurement to 0.01 degree, under the ideal condition of no phase drift or phase jitter during the measurement time, requires the measurement of 10 periods. In practice there is some phase jitter, of the $F - \Delta$ signal in relation to the F signal, produced by the high gain of the AFC loop III of the SCHO which in turn is needed to control frequency over the prescribed range. To compensate for this jitter, 100 periods are measured and the last digit (0.001°) is not displayed. In effect, the displayed value of phase is an average of 100 counts for measurements of phase.

The IF bandwidth of the detector must be as narrow as possible to provide sufficient frequency discrimination and at the same time must be wide enough so that switching transients decay rapidly. The choice of 30 cps bandwidth proved adequate to achieve the aim of 0.01° phase accuracy and permits transients to decay within 0.1 second to a sufficiently low magnitude that accuracy is not affected. As previously described, 0.2 second in the switching time was allowed for transient decay which resulted in a total measurement time of 0.926 second. As previously stated, the phase lock of the SCHO is held to better than 0.01 degree shift in this total measurement time.

If the phase shift being measured is less than the phase shift through the constant phase attenuator, the reverse count will exceed the forward count and the difference will be negative. For a negative number n, however, the timer will indicate 1000.00-n: thus, −15.37° is indicated as 1000.00 − 15.37° or 984.63°. To avoid the necessity for arithmetic subtraction by the operator, the lead-lag switch (Fig. 7) has been provided. The switch reverses the S-X and reference pulse generator inputs to allow the count to appear as a positive number. The operator need only record the indicated count with a change of sign.

If, relative to the reference channel, the total phase shift, through standard or unknown path and through modulators and pulse generators, lies in the neighborhood of 0 or 360 degrees, the phase measuring circuit cannot operate properly. The difficulty is caused by the inability of the timer to respond to pulse pairs having a short time separation. In such

a case the phase circuit will either refuse to cycle or will give highly erratic results. Operation of the zero shift switch (Fig. 7) adds approximately 180 degrees in the reference path. Effectively, then, 180 degrees is added to both S and X measurements and the difference angle is unchanged.

As discussed in Section 2.3, sidebands of 277.78 cps on the signal applied to the phase detector may cause phase measurement error. Similarly, pickup in the detector of 277.78 cps and crosstalk between the two channels in the detector can produce phase error. The components of each channel were mounted in separate shielded compartments and at each point of entry of a power lead into a compartment heavy bypass capacitors were installed. The lead-lag switch required complete shielding including shields between each switch section, grounding of interconnecting wires in their alternate position and the use of shielded cables between the switch and the circuit connecting points.

V. REVERSIBLE TIMER

A block diagram of the reversible timer is shown in Fig. 4. The timer[5] measures the time difference between interval X, the time separation of input pulse pairs when the unknown network is in the measurement circuit, and interval S, the corresponding interval when the phase attenuator is in the circuit.

Input ON and OFF pulses, appearing on the separate input leads from the phase detector (Fig. 7), are applied to an electronic switch whose output is a rectangular pedestal voltage with leading and trailing edges coincident with the leading edges of the ON and OFF pulses. The pedestal voltage is applied to a gate which opens during the pedestal interval and transmits 1 mc voltage to a group of six tandem reversible decades. Reversal of the direction of count is accomplished by the use of interstage gates within the decade counting units actuated from the S-X switch S1B of Fig. 4. An auxiliary $\div$ 100 counter controls the electronic switch so that exactly 100 time intervals are measured for each direction of count.

The above six counting decades, measuring for 100 periods, provide a count to 0.001 degree phase. As described in Section 4.4, this last decade may jitter at random so that the output of only the first five decades are translated to decimal form and transmitted to an in-line readout display.

VI. COMPARISON UNIT

The comparison unit is designed around the parallel comparison type circuit shown in Figs. 3 and 4. The method of detecting the equality in

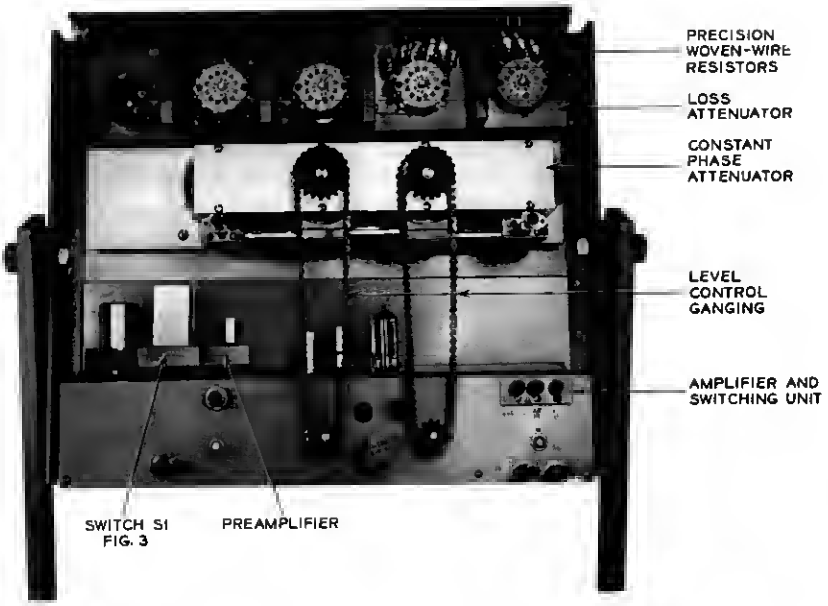

Fig. 9 — Comparison unit, showing the ganged level control.

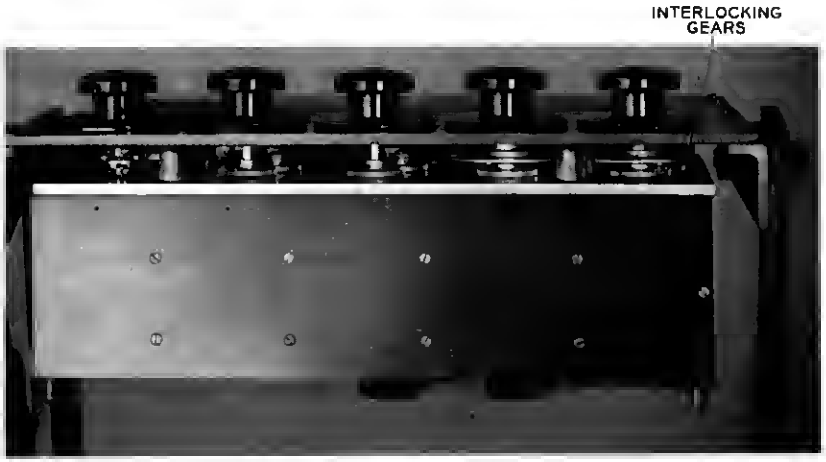

Fig. 10 — Comparison unit, showing ganging of the loss and constant phase attenuators.

magnitude and the difference in phase of the signals from the two paths was discussed in Sections III and IV. The construction used to attain the circuit objectives is shown in Figs. 9 and 10 and some of the special features are described below.

A constant sensitivity of 0.001 db when measuring losses in the range from 0 to 70 db prescribes a constant signal level to the loss detector. This is achieved by the use of step switch gain controls in the wideband amplifier, ganged by chain and sprocket to the attenuator switch shafts, as shown in Fig. 9. As the unknown loss and, therefore, the attenuator loss increases in steps of 1 db and 10 db, the gain of the amplifier is correspondingly increased over a 70 db range, thereby maintaining the level to the detector constant within 1 db.

Measurement of 40 db loss to a sensitivity of 0.001 db corresponds to 0.44 microvolt difference of the signal input to the amplifier and prescribes special precautions to minimize noise and pickup in the amplifier. Power frequency pickup is minimized by operating all heaters on filtered dc and by locating power supplies well away from areas sensitive to 60 cycle field. Microphonics are reduced by shock mounting both the mercury relay S-X switch (S1 of Fig. 3) and the input preamplifier. Thorough shielding and decoupling reduce high frequency crosstalk sufficiently to attain the desired measurement accuracy.

To attain the circuit objectives, the standard attenuator must provide insertion loss in the range of 2 to 122 db adjustable to within 0.001 db for loss measurements and to within 0.1 db for phase measurements. The insertion loss must meet accuracies to nominal of ± 0.001 to 42 db; ± 0.01 to 72 db and ± 0.5 to 122 db at frequencies from 10 to 300 kc. In addition, the insertion phase shift at any setting in the range of 2 to 42 db must be equal to the insertion phase shift at any other setting in that range to within 0.01 degree at any frequency from 10 to 300 kc. The loss accuracies are met with an attenuator embodying precisely adjusted, stable wire-wound resistors; however, the phase shift of this type attenuator varies with setting by as much as 0.5 degree. A second attenuator is used embodying deposited carbon resistors in a semicoaxial structure. Adjustment of internal capacitor trimmers for each step attains the required constant phase shift. The two attenuators are ganged, as shown in Fig. 10, so that the equality in magnitude of the signals from the two circuit arms attained in the loss measurement is held to within 0.1 db for phase measurement and the signal level from either arm to the phase detector is constant to within 1 db for loss of the unknown from 0 to 70 db.

Additional interlocking of the shafts of the 0 to 6 $\times$ 10 db and 0 to

5 × 10 db switches (2 right-hand knobs in Fig. 10) is required to avoid more complicated ganging to the amplifier gain controls. The interlock prevents moving the right-hand knob until the second switch is in the 60 db position, thereby maintaining constant detector input level for losses up to 70 db. Additional amplifier gain for the higher losses added by the right-hand switch is not needed since sensitivity requirements are comparably relaxed.

VII. ACCURACY OF MEASUREMENTS

7.1 *Loss*

The accuracy of loss measurements was verified by measuring a precision 75 ohm attenuator of 0.001 db accuracy. The accuracy of this checking standard was established by first calibrating at dc by measurement of voltage ratios with a precision potentiometer and then measuring the loss change with frequency up to 20 mc using a circuit capable of 0.01 db accuracy. Since for any value up to 40 db the loss change was less than 0.1 db from dc to 20 mc and was linear within the measurement accuracy, by interpolation the loss change of the checking standard should be less than 0.001 db from dc to 200 kc. A typical set of measurements of the checking standard using the 300 kc set is given in Table I.

As shown by the table, the design objectives were met for the measurement set of 0 to 40 db ±0.002 and 40 to 60 db ±0.02.

7.2 *Phase*

The accuracy of phase measurements was verified by comparing phase shift of coaxial cable as measured on the set with values computed from impedance measurements made on a precision bridge.

Western Electric 724 coaxial cable was found to have the necessary

TABLE I

Attenuator Setting (db)	Measured Loss (db) at				
	10 kc	35 kc	105 kc	200 kc	300 kc
14	14.001	14.000	14.000	13.999	13.999
24	23.998	23.998	23.998	23.998	23.998
34	34.000	33.999	33.998	33.998	33.998
44	43.999	43.999	43.998	43.997	43.997
54	54.001	54.001	54.000	53.998	53.996
64	64.002	64.001	63.999	63.993	63.991

time and temperature stability. Open circuit and short circuit impedances were measured on a 1200 foot length of cable. From the bridge measurements input and output image impedances were computed using:

$$Z_i = \sqrt{Z_{oc} Z_{sc}} .$$

Image impedance rather than characteristic or iterative impedance was used since the cable is not exactly symmetrical.

Insertion loss and phase shift between image impedance terminations were computed as follows:

$$\tanh \theta = \sqrt{Z_{sc} Z_{oc}} = U + jV$$

then the insertion loss is

$$\alpha = \tfrac{1}{2} \tanh^{-1} \left[\frac{2U}{1 + U^2 + V^2} \right]$$

and the phase is

$$\beta = \tfrac{1}{2} \tanh^{-1} \left[\frac{2V}{1 + U^2 + V^2} \right].$$

To avoid mismatch effects between cable and the measurement set, L type matching pads were constructed for each calibration frequency. The cable plus pads was measured and then the pads only with the cable removed. The difference in measured values then was recorded as the value of the cable.

A comparison of some measured and computed values is given in Table II.

Some errors inherent in bridge measurement and in constructing impedance matching pads may contribute as much as 0.01 degree of the above 0.03 degree maximum differences. Allowing for this uncertainty, the measurement accuracy of the circuit is considered to be ± 0.02 degree over the frequency range of 70 to 150 kc. Since bridge measurement accuracies at frequencies above 150 kc do not provide sufficient accuracy of calculated phase, further checks were made in the following manner.

TABLE II

Frequency (kc)	Computed (Degrees)	Measured (Degrees)	Difference (Degrees)
70	58.94	58.91	−0.03
90	75.40	75.41	+0.01
120	99.92	99.91	−0.01
130	108.10	108.10	0.00
140	116.26	116.25	−0.01
150	124.30	124.33	+0.03

Four lengths of cable totaling 897 feet were prepared with coaxial fittings. Five impedance isolating pads were prepared each with coaxial fittings such that the cables could be inserted directly between the pads without additional fittings. Measurements of loss and phase were made of the four cable sections in tandem isolated from each other and from the set by pads and then only the pads in tandem were measured. The difference then is the total loss and phase of the four cable sections.

Each individual cable section was measured when terminated with the same pads that terminated the specific section when the tandem measurement was made. Again the pads only were measured, the difference giving the loss and phase of the individual sections.

Values of the measured sum compared to the calculated sum are given in Table III.

The above differences are derived from the individual measurements as outlined above and there is an uncertainty in each measurement of 0.001 db and 0.01 degree which may add in a random manner to 0.003 db and 0.03 degree. Since the above calculated differences are no greater than the random errors, the set capability for measuring a single value is considered to be ± 0.002 db and ± 0.02 degree.

VIII. CONCLUSION

The design effort has been directed toward achieving laboratory precision in measurement and, at the same time, maintaining the ease of use and speed necessary for a large volume of measurements. The entire frequency range of the set described in this article is covered without band switching by the use of a heterodyne signal oscillator which provides good frequency accuracy by locking to a frequency standard. The need for manual detector tuning is eliminated through the use of frequency conversion employing a locked slave (or offset) frequency source to provide a constant detection frequency. The desired test frequency can be set and read directly from the markings of a film scale type master oscillator and the dials of an interpolation oscillator. The insertion loss and

TABLE III

	150 kc		300 kc	
	Loss	Phase	Loss	Phase
Measured	0.872	79.46	1.179	156.67
Calculated	0.875	79.44	1.178	156.64
Difference	0.003 db	0.02 deg.	0.001 db	0.03 deg.

phase of an unknown may be read directly from the dials of an attenuator and from an in-line digital readout, respectively, and since the system zero is independent of test frequency, no circuit zero is required.

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APPENDIX

Limitations of Frequency Modulation in SCHO Oscillator

The introduction of errors in phase measurement by frequency modulation of tbe F and $F - \Delta$ frequencies of Fig. 6 was discussed in Section 2.3. The derivation of the limitation of the amplitude of a spurious modulating signal is as follows:

The output of a frequency-modulated oscillator of very low modulation index (m_f) contains only one pair of sidebands and is well known (see Ref. 6 and similar texts) to be expressed as

$$e = E_0\left[J_0\left(\frac{\Delta f}{f_m}\right)\sin \omega t + J_1\left(\frac{\Delta f}{f_m}\right)[\sin(\omega + p)t - \sin(\omega - p)t]\right] \quad (1)$$

where

Δf = frequency deviation

f_m = modulating frequency

$J_n\left(\frac{\Delta f}{f_m}\right)$ = Bessel function of the first kind, order n.

For $\frac{\Delta f}{f_m}$ near zero (1) reduces to

$$e = E_0\left(\sin \omega t + \frac{\Delta f}{2f_m}[\sin(\omega + p)t - \sin(\omega - p)t]\right)$$

The maximum phase modulation is then:

$$\Delta\psi = 2f_m/\Delta f$$

but

$$\Delta f = kv_m$$

where

k = reactance tube oscillator sensitivity in cps per volt

$= 2.3 \times 10^3$ cps/volt for $F5$ (Fig. 6)

v_m = amplitude of modulating voltage

thus

$$\Delta\psi = \frac{f_m}{1.2 \times 10^3 v_m}.$$

For a phase error of 0.01 degree, $\Delta\psi = 0.01 \times (\pi/180)$ radians. Hence, the ratio of carrier to sideband amplitude must be greater than

$$\frac{1}{\Delta\psi} = 5.7 \times 10^3 \quad \text{or} \quad 75 \text{ db}$$

and for $f_m = 278$ cps, the maximum allowable modulating voltage is

$$v_m = \frac{278}{1.2 \times 10^3 \times 5.7 \times 10^3} = 40 \text{ microvolts.}$$

REFERENCES

1. Alsberg, D. A. and Leed, D., A Precise Direct Reading Phase and Transmission Measuring System for Video Frequencies, B.S.T.J., **28**, April, 1949, pp. 221–238.
2. Slonczewski, T., Precise Measurement of Repeater Transmission, Elec. Engr., **73**, April, 1954, pp. 346–347.
3. Slonczewski, T., Measuring Apparatus, United States Patent 2,666,100.
4. Israel, J. O., United States Patent 2,987,680.
5. Barney, K. H., The Binary Quantizer, Elec. Engr., **68**, November, 1949, pp. 962–967.
6. Terman, F. E., *Radio Engineering*, 3rd Ed., McGraw-Hill, New York, 1947.